Project 1 checklist:

Your report should contain these items from the various parts of the project. Please submit as a single file, either as a MS Word file, a PDF file, or a .zip archive.

Xilinx Lab1: (40 points)

1. Step 1: (10 points)
   1. Screen capture of spectrum plots of the initial waveforms
   2. Screen capture of spectrum plots after adding Digital FIR Filter block
   3. Screen capture of resource utilization output
   4. Screen capture of final block diagram
   5. Compare your results with the tutorial results and note any differences or if the same.
2. Step 2: (10 points)
   1. Screen capture of resource utilization output for higher frequency in Generate step
   2. Compare your results with the tutorial results and note any differences or if the same.
3. Step 3: (10 points)
   1. Screen capture of final block diagram using discrete components
   2. Screen capture of spectrum plots
   3. Screen capture of resource utilization output
   4. Compare your results with the tutorial results and note any differences or if the same.
4. Step 4: (10 points)
   1. Part 1, Screen capture of spectrum plots of floating-point version
   2. Part 1, Screen capture of floating-point resource utilization output
   3. Part 1, Compare your results with the tutorial results and note any differences or if the same.
   4. Part 2, Screen capture of scope results for fixed-point version – initial version
   5. Part 2, Screen capture of scope results for fixed-point version – after changing reinterpret and convert blocks
   6. Part 2, Screen capture of fixed-point resource utilization output
   7. Part 2, Compare your results with the tutorial results and note any differences or if the same.

Xilinx Lab2: (15 points)

1. Step 1: (8 points)
   1. Include your state\_machine.m code
   2. Screen capture of final block diagram
   3. Screen capture of output waveform
   4. Compare your results with the tutorial results and note any differences or if the same.
2. Step 2: (7 points)
   1. Screen capture of final block diagram
   2. Screen capture of final output waveform
   3. Compare your results with the tutorial results and note any differences or if the same.

Xilinx Lab3: (15 points)

1. Step 1: (10 points)
   1. Screen capture of timing analyzer results – realize that the Kintex -3 part will have less timing error than the Zynq Artix -1 part
   2. Modify latency in various blocks in order to pass timing. This may be different than the suggestion in the tutorial. Explain your process.
   3. Screen capture of timing analyzer results – passing – after modifications
2. Step 2: (5 points)
   1. Screen capture of resource analyzer results for the Zynq Artix chip
   2. Compare your results with the tutorial results and note any differences or if the same.

CUDA Lab: (30 points)

1. (5 points) Screen capture of debug results window for arraySize = 10, threads = size, blocks = 1 initial parameters
2. (10 points) Include table of results for all of the arraySize values listed in the problem: 100, 200, 500, 750, 1000, 1250, 1500, 2000, 5000, 10000, 25000, and 64000. Table should record: Performance in Mops/s, Time, Size, Threads, Blocks, and Total Threads
3. (2 points) What happens at arraySize = 1250 with the original threads and blocks value? Explain.
4. (2 points) Screen capture of the Debug results for arraySize = 25000
5. (2 points) Final two values of variable c at 64000 with minimum threads and blocks set for 25000. How did you fix these values.
6. (4 points) Analyze your table for the percentage increase in performance, time, and size
7. (5 points) Include final Proj1\_kernel.cu file